(11) Patent Publication number: 2-100506
(19) Japanese Patent Office (JP)
(12) Publication Patent Official Report (A)
(43) Date of publication of application: 12.04.1990
(51) Int. Cl.[5] Identification sign Patent Office reference number:

H 03 G 3/20	C	8221 – 5J
3/00	B	8221 – 5J
3/20	A	8221 – 5J

Patent claims amount: no claim; claim paragraph amount: 1
(8 pages in all)

.....

(54) **Title of the invention: AUTOMATIC GAIN CONTROL CIRCUIT**

(21) Application number: 63-253424
(22) Date of filing: 07.10.1988

(71) Applicant:
FUJITSU LTD
(72) Inventor:
TOZAWA YOSHIHARU
(72) Inventor:
UCHIJIMA MAKOTO
(72) Inventor:
YUDA TSUTOMU
(74) Agent: patent attorney:

SPECIFICATIONS

1. Title of the invention:

Automatic Gain Control Circuit

2. Field of Patent Claims:

An automatic gain control circuit comprises:

A variable gain amplifier (1) for variably adjusting a signal level of a reception signal;

A level detector (2) for detecting a signal level of the reception signal adjusted by the above-mentioned variable gain amplifier (1);

A comparator (3) for requiring a value difference between the signal level detected by the above-mentioned level detector (2) and an objective signal level;

A loop filter means (4) for practicing a new process with a new self output value adding the self output value to the said value difference required by the above-mentioned comparator (3);

An initial value setting circuit (5) for setting an initial value of an output value in the above-mentioned loop filter means (4).

The automatic gain control circuit performs a process to adjust the signal level of the reception level to an objective level by controlling a gain of the above-mentioned variable gain amplifier (1) following the value outputted from the above-mentioned loop filter means (4) during reception of the reception signal.

The automatic gain control circuit uses a value in which a time required for adjustment to an objective signal level comes almost equal to a maximum reception

signal level and a minimum reception signal level within a gain control range as the initial value set by the above-mentioned initial value setting circuit (5).

3. Detailed explanation of the Invention:

[Outline]

The automatic gain control circuit performs a process to adjust the reception signal to a fixed signal level during the reception of the reception signal.

The purpose of the automatic gain control circuit is to realize an adjusting processing in a shorter time by using a value in which a time required for adjustment to an objective signal level comes almost equal to a maximum reception signal level and a minimum reception signal level within a gain control range as the initial value set by the above-mentioned initial value setting circuit. An automatic gain control circuit comprises: a variable gain amplifier for variably adjusting a signal level of a reception signal; a level detector for detecting a signal level of the reception signal adjusted by the above-mentioned variable gain amplifier; a comparator for requiring a value difference between the signal level detected by the above-mentioned level detector and an objective signal level; a loop filter means for practicing a new process with a new self output value adding the self output value to the said value difference required by the above-mentioned comparator; an initial value setting circuit for setting an initial value of a value outputted from the above-mentioned loop filter means. The automatic gain control circuit performs a process to adjust the signal level of the reception level to an objective level by controlling a gain of the above-mentioned variable

gain amplifier following the value outputted from the above-mentioned loop filter means during reception of the reception signal.

[Technical Field]

The present invention relates to an automatic gain control circuit which performs a process to adjust a reception signal to a fixed signal level during reception of a reception signal, especially, it relates to an automatic gain control circuit capable of realizing an adjusting processing in a shorter time.

In a digital satellite communication used TDMA (time division multi connection), generally, a data communication is performed following a burst signal. To create a system which modulates greater data from one burst signal a modulator is required to be input into stabile operation in a shorter time. Thus, even if there is an automatic gain control circuit which adjusts a signal level of a reception signal of the burst signal, it should be constituted such to make it possible adjusting to a predetermined fixed level in a shorter time.

[Technique of the Prior Art]

The automatic gain control circuit prepares the variable gain amplifier which variably adjusts the signal level of the reception signal, requires a value difference between the signal level of the received signal adjusted by this variable gain amplifier and the objection signal level, and filters this value difference by the loop filter. Then the automatic gain control circuit adjusts the signal level of the reception signal to the objective signal level by controlling the gain of the variable gain amplifier following the output value in this loop filter.

In the automatic gain control circuit with such a constitution in accordance with the prior art the output value in the loop filter when input of the burst signal is used, namely, an initial value of output in the loop filter is set to adjust the output level in the variable gain amplifier to objective signal level when the reception signal of objective signal level is input.

[The problem which the present invention intends to solve]

However, in such a prior technique there is a problem that a time required for adjustment a signal level of the reception signal to an objective signal by characteristics of the level detector for detecting an output level in the variable gain amplifier and amplifier decrease characteristic of the variable gain amplifier is not shortest to be optimum within a range of all signals level of the reception signal.

In accordance with a concrete explanation in a prior technique there is also a problem that a comparatively long time is required for adjustment process when smaller signal level than an objective signal level is inputted in opposition to that an adjust process is completed at a comparatively short time when bigger signal level than an objective signal level is inputted. Thus, in the prior technique a time required for performing a stabile modulation process is long. Consequently, there is a disadvantage that a number of data included into the signal with the same burst length is small.

In accordance with the present invention an automatic gain control circuit performs a process to adjust a reception signal to a fixed signal level during reception of a reception signal. The purpose of the present invention is to offer an automatic gain control circuit capable of realizing an adjusting processing in a shorter time.

[Means for solution to the problem]

FIGURE 1 is a diagram showing a principle of constitution of the present invention.

In the FIGURE 1 is a variable gain amplifier for variably adjusting a signal level of a reception signal; 2 is a level detector for detecting a signal level of the reception signal adjusted by the variable gain amplifier 1; 3 is a comparator for requiring a value difference between the signal level detected by the level detector 2 and an objective signal level; 4 is a loop filter means for practicing a new process with a new self output value adding the self output value to the value difference required by the comparator 3; 5 is an initial value setting circuit for setting an initial value of an output value in the loop filter means 4; 7 is a clock circuit for transmitting a clock which determines a new process for the loop filter means 4. Thus, a control for a gain of the variable gain amplifier 1 is performed following an output value in the loop filter means 4.

[Action]

In the present invention if a reception state inform signal which shows a state when the reception signal is input is output, the loop filter means 4 follows the clock

from the clock circuit 7 and performs a process of a sequential update of self output value as a starting point of initial value set by the initial value setting circuit 5. The variable gain amplifier 1 follows an output value of this loop filter means 4 and controls the adjustment of the signal level of the reception signal into the objective predetermined fixed level. At this time a value in which a time required for adjustment to an objective signal level comes almost equal to a maximum reception signal level and a minimum reception signal level with in a gain control range as the initial value set by the initial value set circuit 5 is used.

Thus, in accordance with the prior technique, a time required for adjustment process completion can not be greatly changed to a maximum reception signal level and a minimum reception signal level, therefore, the signal level of the reception signal can be adjusted to the predetermined objective level in overage at a short time.

[An example of the preferred embodiment]

The present invention will be described further below referring to the example of the preferred embodiment. FIGURE 2 shows a constitution of the preferred embodiment of an automatic gain control circuit according to the present invention. In the FIGURE the numbers are the same with that of the FIGURE 1. 1a is a gain control terminal which provides the variable gain amplifier 1 is a terminal for inputting an analog voltage set an amplifying rate of the variable gain amplifier 1, 6 is a reception detecting circuit for outputting a reception state inform signal which shows the state when the reception signal is input, 8 is a mixing circuit connected to

the variable gain amplifier 1 for frequency-converting the reception signal the level of which is controlled by the variable gain amplifier 1 into a signal of a base band, 9 is a filter connected to the mixing circuit for extracting components with a high frequency to be turned back to a low frequency by a sampling, 10 is an A/D converter connected to the filter 9 for converting the reception signal into a digital value synchronizing to the clock signal from the clock circuit 7, 11 is a digital filter connected to the A/D converter for changing a digital value converted by the A/D converter into a digital value of a wave form, 12 is a D/A converter connected to the loop filter means 4 for converting a digital output of the loop filter means 4 into an analog voltage and then for inputting it to the gain control terminal 1a.

FIGURE 3 shows a detailed constitution of a preferred embodiment in accordance with a loop filter means. In the FIGURE, 40 is a D type flip flop circuit for performing a process to turn back an output value to an input value synchronizing to the clock signal from the clock circuit 7 and for performing a process to set an integral to "0" before performing the setting of an initial value when a reception state inform signal from the reception detecting circuit 6 is input, 41 is the first integral input unit for requiring an additional value between an input value inputted to the loop filter means 4 and an output value turned back through the D type flip flop circuit 40, 42 is the second integral input unit for requiring an additional value between an initial value set by the initial value setting circuit 5 and an output value of the first integral input unit 41. Thus, in this preferred

embodiment the initial value setting circuit 5 performs a process for setting an initial value to the second integral input unit 42 only when the reception state inform signal is input, namely, in case of adjustment of the signal level of the reception signal. Consequently, the second integral input unit 42 realizes an additional process only at this time.

The loop filter means 4 operates to sequentially update a self output value as a starting point of an initial value set by the initial value setting circuit 5 following to the clock from the clock circuit 7 by using such a constitution. Thus, in the FIGURES 2 and 3 wiring number or the like is prepared adjusting to decomposition state of the digital value. It is omitted in the FIGURES for convenience.

Following, an adjustment process of a signal level of an automatic gain control circuit constituted in such a way will be described further below.

If the reception state inform signal which shows the state when the reception signal is input from the reception detecting circuit 6 is input, the D type flip flop circuit 40 sets an integral to "0", the initial vale setting circuit 5 inputs an initial value being previously selected should be input into adjusting processing of the signal level into the second integral input unit 42, synchronizing to it. Thus, an initial value inputted into the second integral input unit 42 is input into the gain control terminal 1a by being converted into an analog voltage by D/A converter 12 and then is set into the value utilized an amplification rate of the variable gain amplifier 1. Then, A/D converter 10 performs a process for converting the reception signal

amplified by the variable gain amplifier 1 to a sequential digital value follo wing the clock from the clock circuit 7.

In accordance with a comparison of the comparator 3 when it is determined whether the signal level detected by the level detector 2 is bigger then an objective value, the first integral input unit 41 performs a process for converting the big value difference into this output value of adding to the previous output value in each time when the clock from the clock circuit 7 is input. Consequently, for example if the initial value is "50", the output value outputted from the second integral input unit 42 is sequentially amplified to, for example, from "50" becomes "65" ? "78" ? "91" ? "100". The variable gain amplifier 1 performs a process for reducing an amplification rate adjusting to an addition of the output value of this second integral input unit 42, therefore, the signal level outputted by the variable gain amplifier 1 is concluded into an objective value being sequentially reduced, at the end, "0" is output from the comparator 3. Then, the output value of the second integral input unit 42 is concluded into a greater predetermined value than the initial value (it is determined by the signal level of the reception signal).

In opposite, in accordance with a comparison of the comparator 3, when it is determined whether the signal level detected by the level detector 2 is smaller then an objective value, the output value outputted by the second integral input unit 42 is sequentially reduced from the initial value, the variable gain amplifier 1 performs a process to increase an amplification rate adjusting to the reduction of the output value of the second integral input

unit 42. In accordance with this process, the signal level outputted by the variable gain amplifier 1 is concluded into an objective value being sequentially amplified, at the end, "0" is outputted from the comparator 3, and the output value of the second integral input unit 42 is concluded into predetermined smaller value then an initial value.

Following, the value o an initial value set by the initial value setting circuit will be described further below referring to the FIGURE 4 and FIGURE 5 which show an experimental result of a time required for conclusion.

FIGURE 4 is an experimental result when a value at which the signal level of an objective value is outputted by the variable gain amplifier 1 is used when the reception signal of the signal level which is an objective value is received as an initial value. In the FIGURE axis of abscissa shows a number of sampling times of the signal level, axis of Y shows a control value code for output value outputted from the second integral input unit 42. Thus, the result of experiment is represented by a straight line at the part at which a control code value has a fixed value for convenience. Characteristics of the FIGURE 4 is the technique of the prior art. In accordance with an explanation of the unit [**The problem which the present invention intends to solve**], when the signal level which is bigger then an objective signal is input, adjusting processing is completed in comparatively short time with 15 time rate, but when the signal level which is smaller then an objective signal level is inputted, there is a problem that a comparatively long time is required for adjusting with 33 time rate.

Thus, in the present invention as shown in FIGURE 5 an initial value is shifted and adjusting processing is realized by using a value in which a time required for adjustment into an objective signal level comes almost equal to a maximum reception signal level and a minimum reception signal level within a gain control range as the initial value. Thus, in FIGURE 5 an experimental result is represented by a straight line in one part for convenience.

FIGURE 5 is an experimental result when "50" which is smaller then "70" in the prior technique is adopted as a control value code of the initial value. Thus, the amplification rate of the variable gain amplifier 1 determined by the initial value is set a little higher than that in the prior technique, a time required for adjustment becomes shorter by making a time required for adjustment to an objective signal level almost equal to a maximum reception signal level and a minimum reception signal level within a gain control range. Thus, in the example of FIGURE 5 when the signal level bigger than an objective signal level is input, a long time is required for adjusting than that of the prior technique with 20 time rate, when the signal level smaller than an objective signal level is input, a time required for adjustment can be shorter than that of the prior technique with 25 time rate. If the initial value becomes smaller, an item of the value of these two ranges is compressed. However, if the initial value becomes to small, a long time is required for adjustment when the signal level smaller than an objective signal level is input.

FIGURE 6 shows a constitution of another preferred embodiment in accordance with the loop filter means 4. FIGURE 6 (A) shows an example of the preferred embodiment at which the loop filter means 4 is constituted establishing an integral where the initial value from the initial value setting circuit 5 is added to an input side of an original loop filter means 4. FIGURE 6 (B) shows an example of the preferred embodiment at which the loop filter means 4 is constituted establishing an integral where the initial value from the initial value setting circuit 5 is added to an output side of an original loop filter means 4.

Thus, in the example of the preferred embodiment shown in FIGURE 6 (A), the initial value setting circuit 5 performs a process for setting the initial value to the integral only when an input of the reception signal is detected by the reception detecting circuit 6, but in the example of the preferred embodiment shown in FIGURE 6 (B), the initial value setting circuit 5 performs a process for setting the initial value to the integral output during adjusting processing. By using such a constitution, the loop filter means 4 performs a process for sequentially updating self output value with an initial value which the initial value setting circuit 5 sets as a starting point in accordance with a clock from the clock circuit 7. The loop filter means 4 can realize a process by using an analog signal. In this time, the loop filter means 4 obtains the initial value from the initial value setting circuit 5 by an analog signal. In such a case, the predetermined embodiment of the initial value setting circuit and the integral operates as shown in FIGURE 7.

The present invention was explained above; therefore, the present invention is not limited by it. For example, in the explanation of the preferred embodiment it is described that an output value of the loop filter means becomes bigger, therefore, an amplification rate of the variable gain amplifier is reduced, but it is also possible to be constituted in an opposite way.

[Results of the present invention]

Thus, in accordance with the present invention an adjusting processing can be realized in a shorter time in the automatic gain control circuit which performs a process to adjust the reception signal to the fixed signal level during signal reception. Therefore, a greater data amount can be transmitted by the burst signal with the same burst length.

[Brief description of the drawings]

FIGURE 1 is a diagram showing a principle of constitution of the present invention;

FIGURE 2 is a diagram showing a constitution of a preferred embodiment in accordance with the present invention;

FIGURE 3 is a diagram showing a constitution of a preferred embodiment in accordance with a loop filter means;

FIGURE 4 and FIGURE 5 are diagrams showing an explanation for set initial values;

FIGURE 6 is a diagram showing a constitution of another preferred embodiment in accordance with a loop filter means;

FIGURE 7 is a diagram showing a constitution of a preferred embodiment for an initial value setting.

[Description of Numbers]

1 is a variable gain amplifier;
1a is a gain control terminal;
2 is a level detector;
3 is a comparator;
4 is a loop filter means;
4a is a loop filter;
5 is an initial value setting circuit;
6 is a reception detecting circuit;
7 is a clock circuit;
8 is a mixing circuit;
9 is a filter;
10 is an A/D converter;
11 is a digital filter;
12 is a D/A converter;
40 is a D type flip flop circuit;
41 if the first integral input unit;
42 is the second integral input unit.

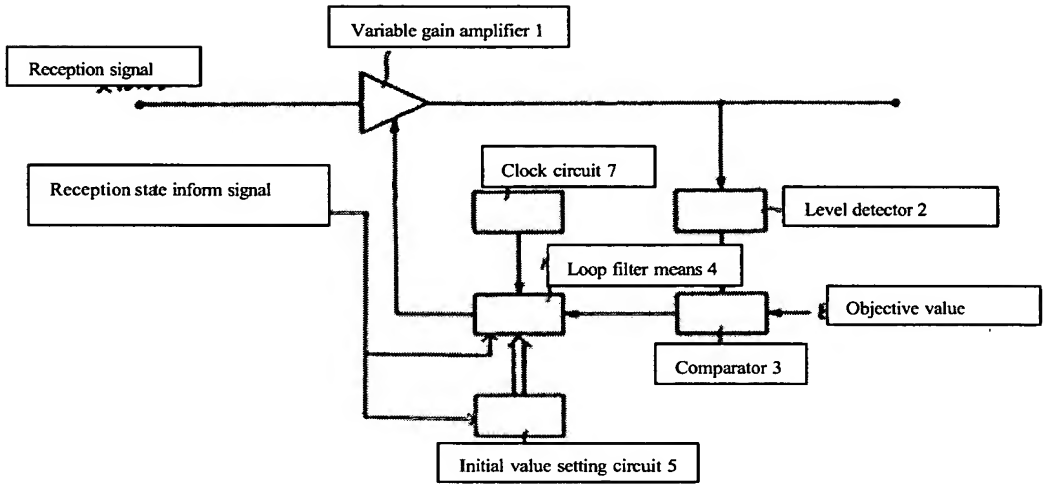


FIGURE 1 is a diagram showing a principle of constitution of the present invention

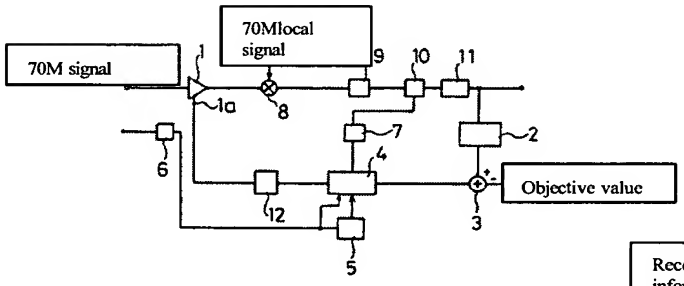


FIGURE 2 is a diagram showing a constitution of a preferred embodiment in accordance with the present invention

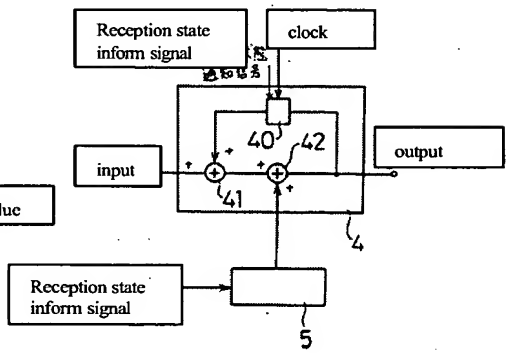


FIGURE 3 is a diagram showing a constitution of a preferred embodiment in accordance with a loop filter means

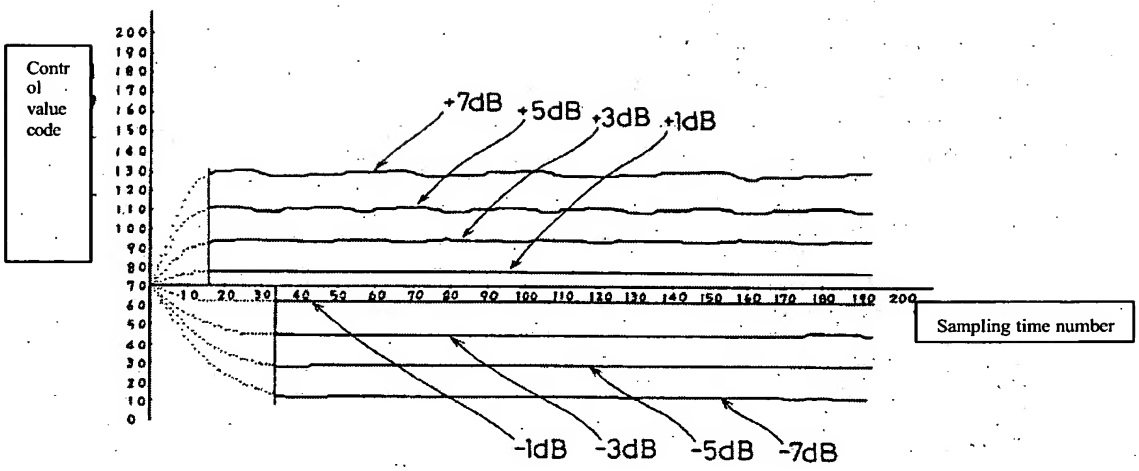


FIGURE 4 is a diagram showing an explanation for set initial values (I)

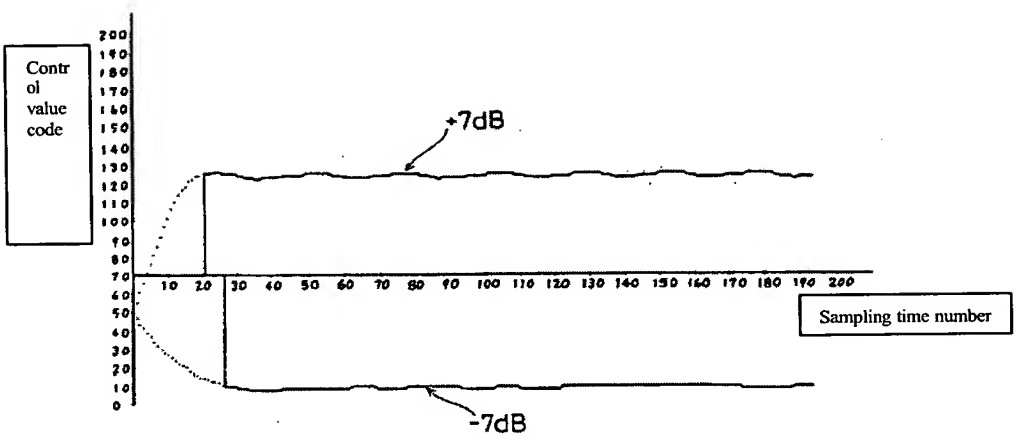
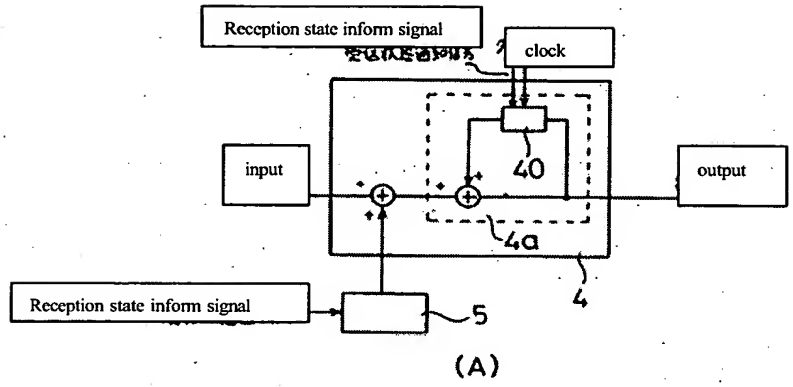


FIGURE 5is a diagram showing an explanation for set initial values (II)



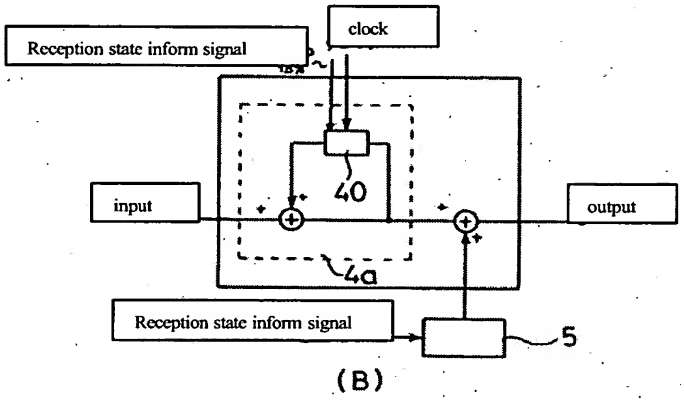


FIGURE 6 is a diagram showing a constitution of another preferred embodiment in accordance with a loop filter means;

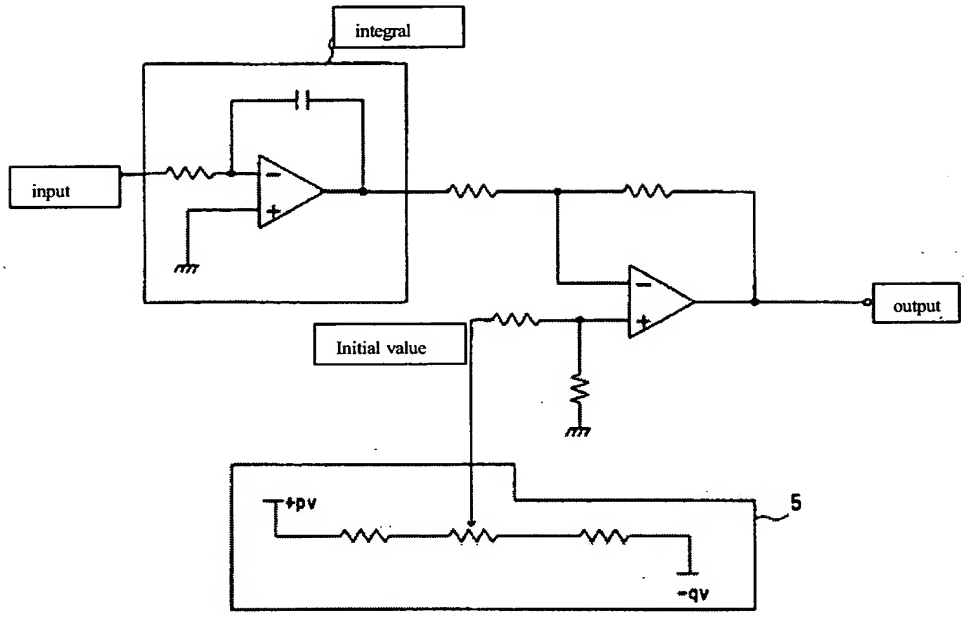


FIG.7 is a diagram showing a constitution of a preferred embodiment for an initial value setting